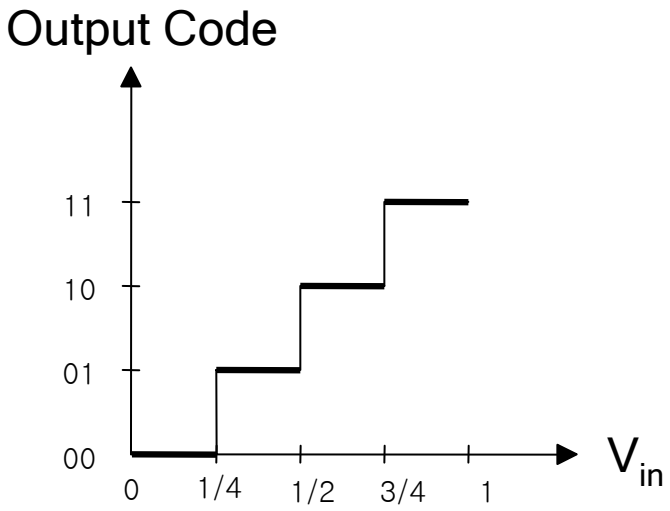
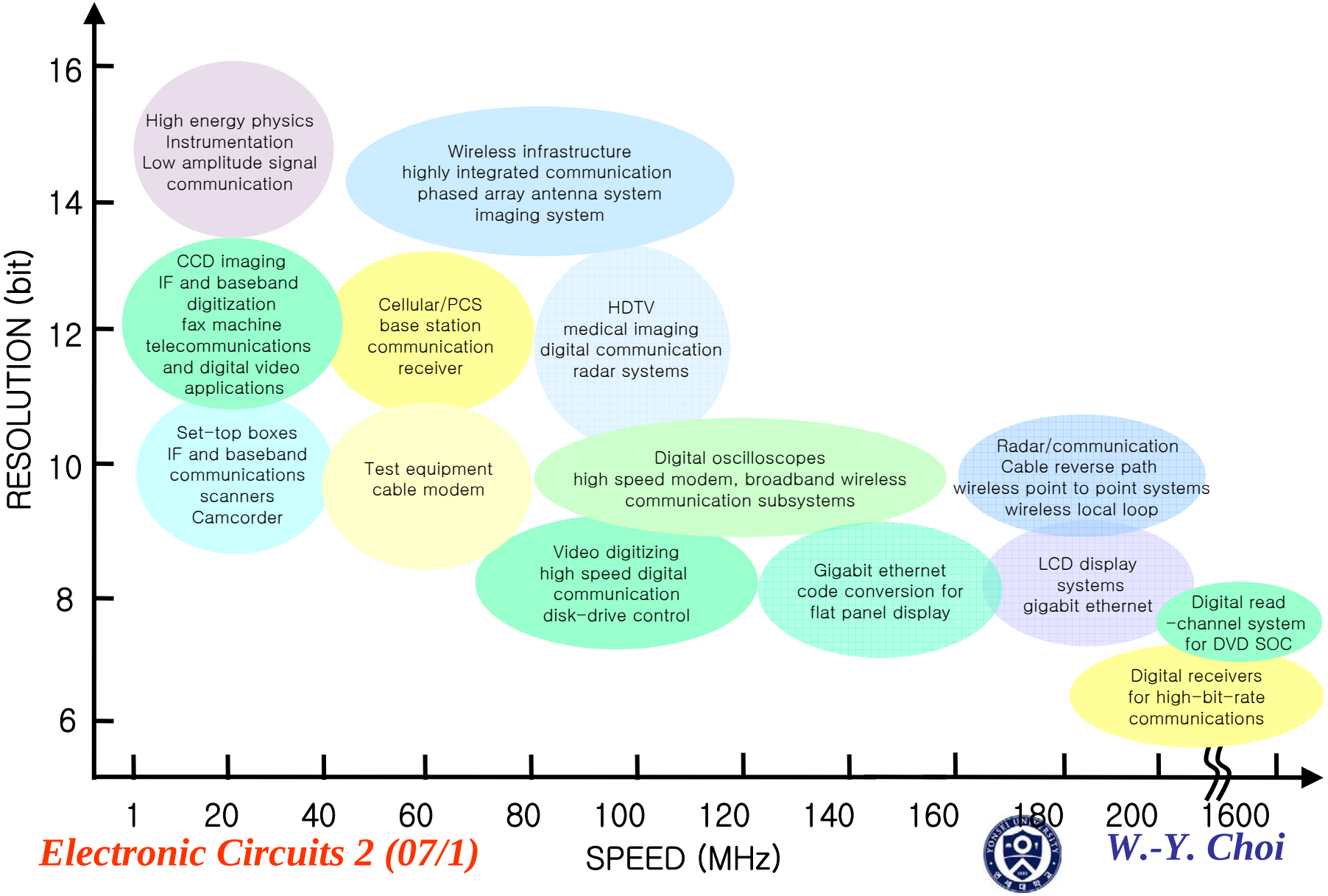
Lect. 25: Analog-to-Digital Converters



Many ADC architectures are available

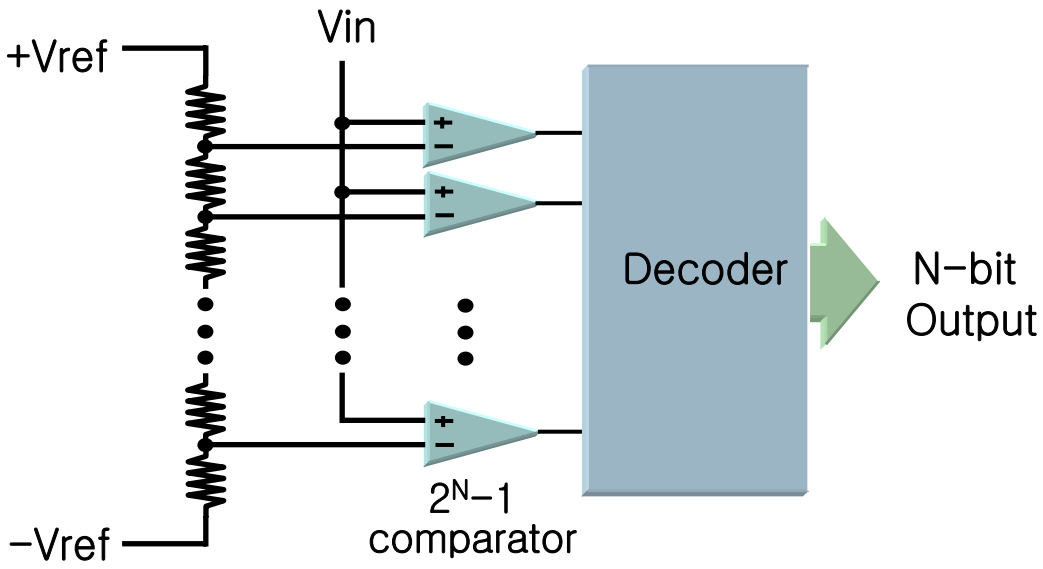
Lect. 25: Analog-to-Digital Converters



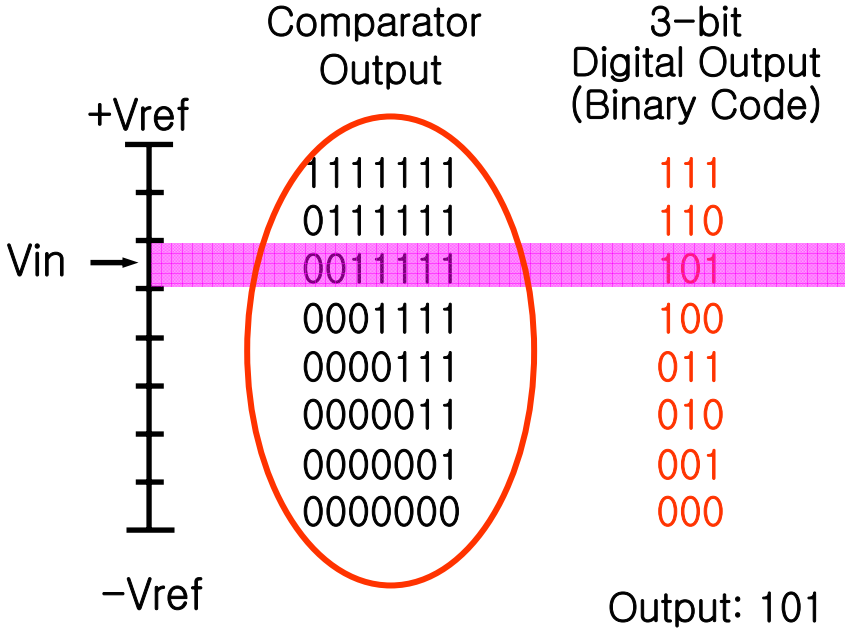
W.-Y. Choi

Lect. 25: Analog-to-Digital Converters

Flash ADC



Ex.) 3−bit Flash ADC



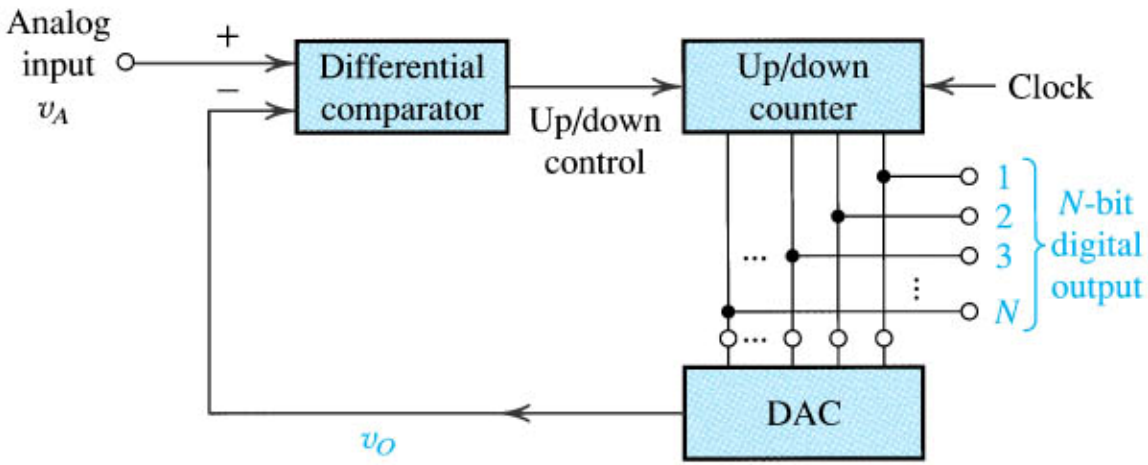
Thermometer Code

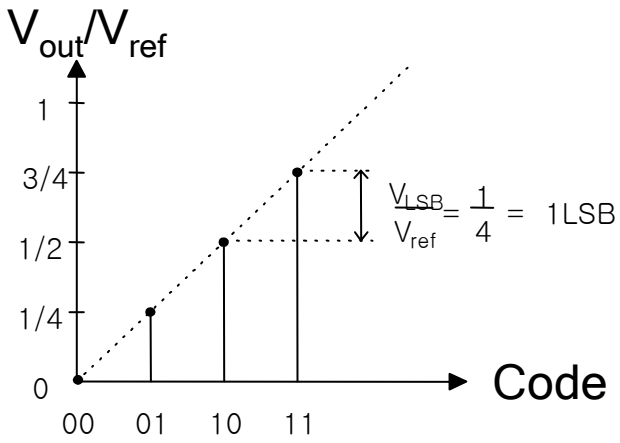
Fast because of parallel processing

R matching problem ➔ Expensive, High-performance applications

Lect. 25: Analog-to-Digital Converters

Feedback-Type ADC



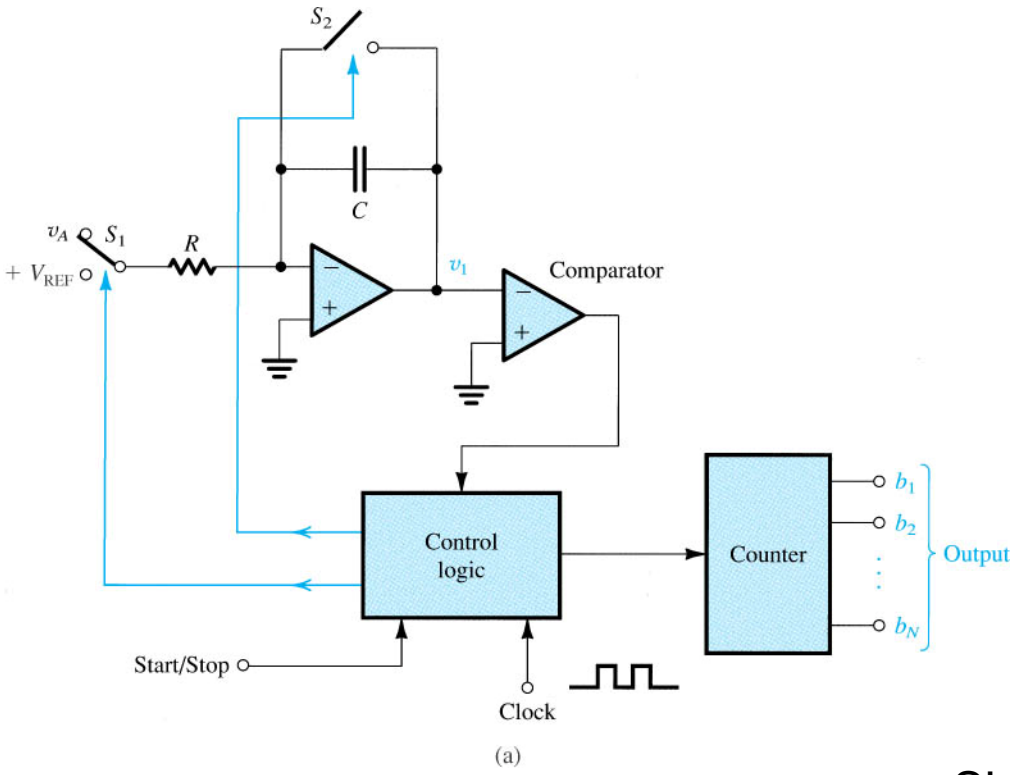


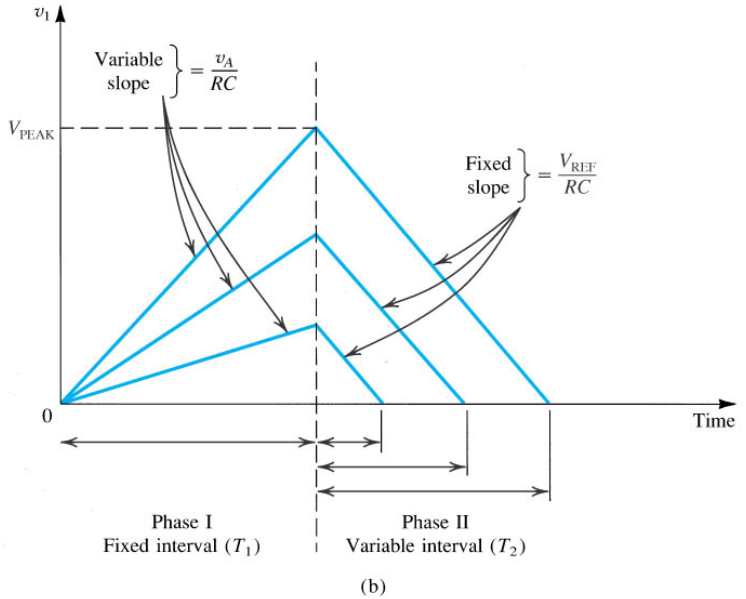
Count up DAC
Until DAC output matches analog input

Very simple but not for high performance

Lect. 25: Analog-to-Digital Converters

Dual-Slope ADC





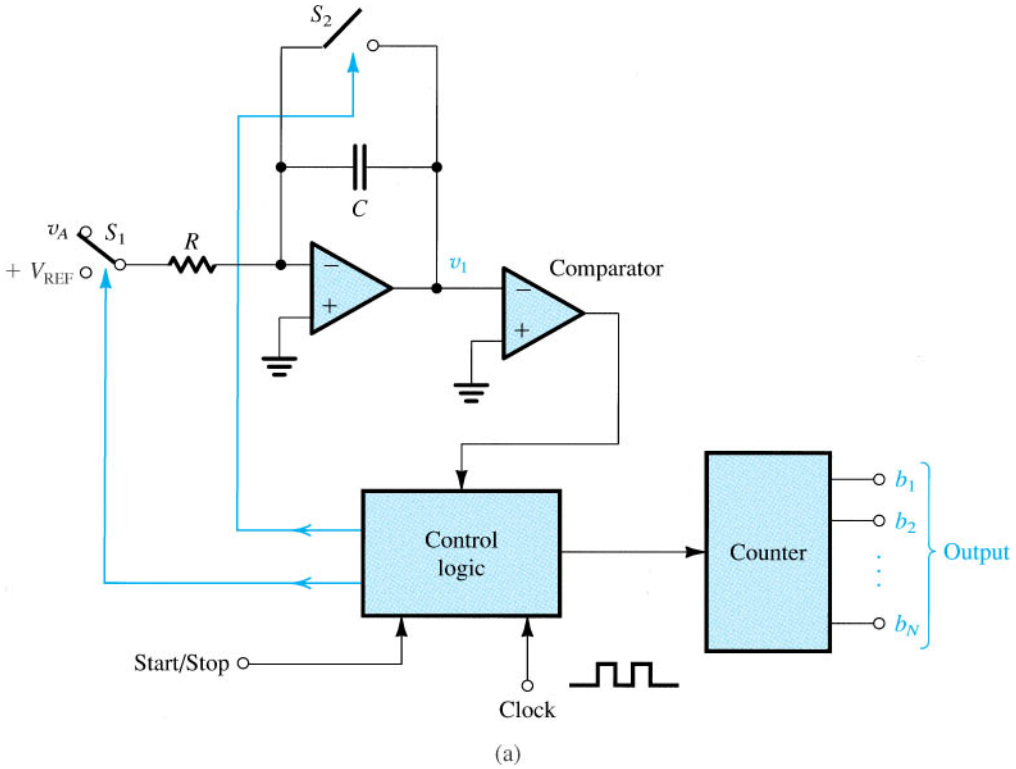
Charge up the integrator for T_1 with v_A

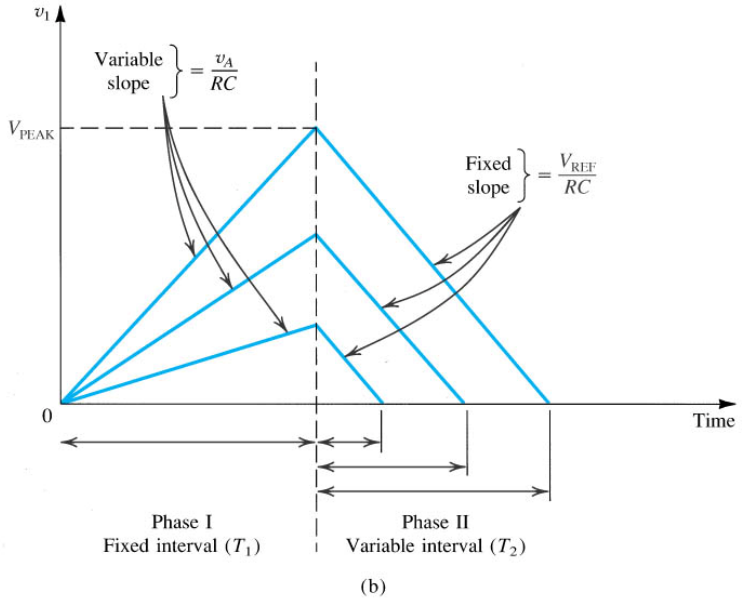
$$V_{PEAK} = \frac{v_A}{RC} \cdot T_1$$

Simultaneously count up the counter to 2^N

Lect. 25: Analog-to-Digital Converters

Dual-Slope ADC





Discharge the integrator with V_{REF}
Stop counting when v_I reaches 0 at T_2

$$V_{PEAK} = \frac{V_{REF}}{RC} \cdot T_2$$

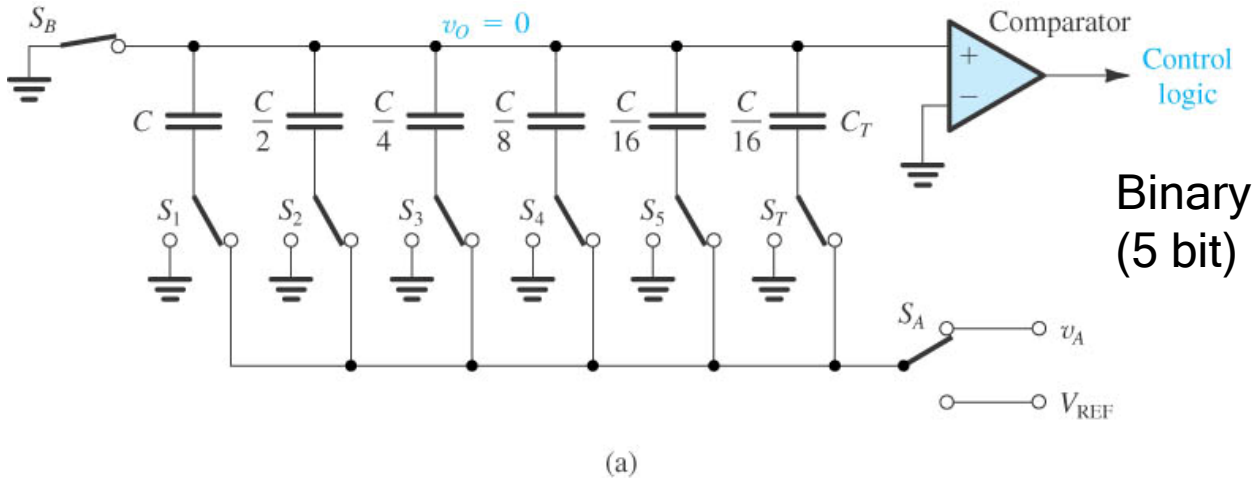
$$\therefore T_2 = T_1\left(\frac{v_A}{V_{REF}}\right) \Longrightarrow n = 2^N\left(\frac{v_A}{V_{REF}}\right)$$

High accuracy: No direct dependence on R, C

But slow

Lect. 25: Analog-to-Digital Converters

Charge Redistribution ADC



(a)

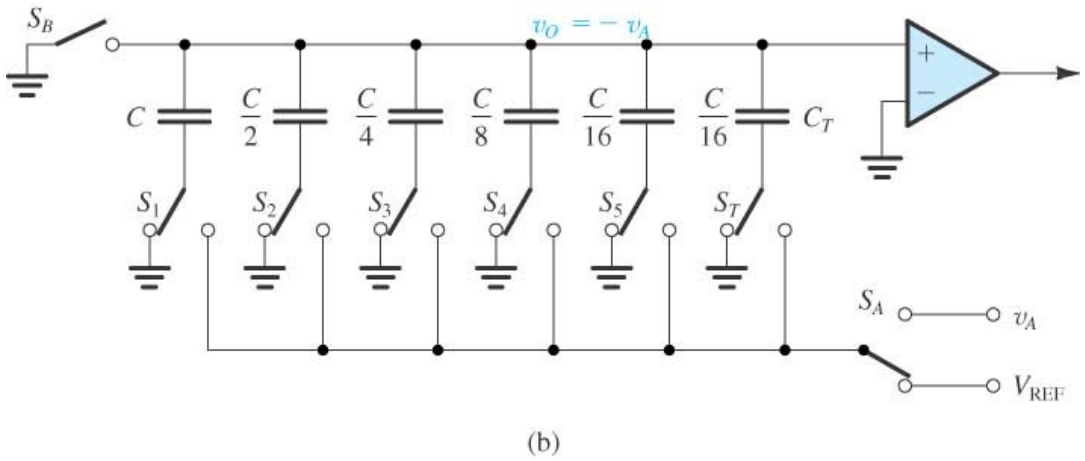
Binary Weighted C
(5 bit)

Sampling Phase

$Q_{total} = 2\ C\ v_A$

Lect. 25: Analog-to-Digital Converters

Charge Redistribution ADC



(b)

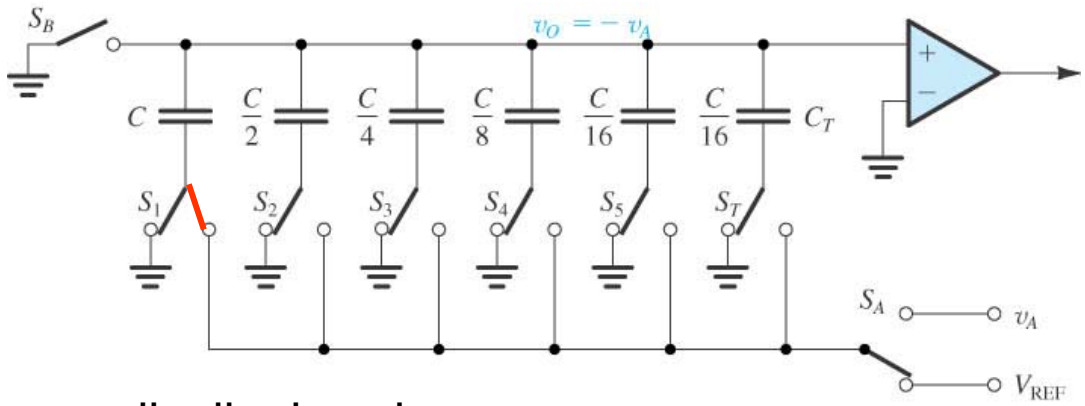
Hold Phase

$v_O = - v_A$

S_A connect to V_{REF}

Lect. 25: Analog-to-Digital Converters

Charge Redistribution ADC



Charge-redistribution phase

With S_1 connected to V_{REF}, $v_O = V_{REF}/2 - v_A$

If $v_o > 0$, connect S_1 to ground and move to S_2

If $v_o < 0$, move to S_2

Repeat above with increasing n

Final switch configuration is the digital output